Docket: GS 145 D1

CLAIMS:

1. A trench DMOS transistor device comprising:

a substrate of a first conductivity type, said substrate acting as a common drain region for said device;

an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

an insulating layer lining at least a portion of said trench;

a conductive region within said trench adjacent said insulating layer;

a body region of a second conductivity type provided within an upper portion of said epitaxial layer and adjacent said trench;

a source region of said first conductivity type within an upper portion of said body region and adjacent said trench; and

a low resistivity deep region extending into said device from an upper surface of said epitaxial layer, said low resistivity deep region acting to provide electrical contact with said substrate.

2. The trench DMOS transistor device of claim 1, wherein said low resistivity deep region has a resistivity of 0.01 Ohm-cm or less and extends at least 20 % of the distance from said upper surface of said epitaxial layer to said substrate.

3. The trench DMOS transistor device of claim 1, wherein said deep region comprises a semiconductor region of said first conductivity type.

4. The trench DMOS transistor device of claim 3, wherein said deep region extends all the way to said substrate.

5. The trench DMOS transistor device of claim 1, wherein said deep region comprises a metallic region.

6. The trench DMOS transistor device of claim 5, wherein said metallic region comprises aluminum.

7. The trench DMOS transistor device of claim 5, wherein said deep region extends all the way to said substrate.

8. The trench DMOS transistor device of claim 1, wherein said deep region comprises a doped polysilicon region.

9. The trench DMOS transistor device of claim 8, wherein said deep region extends all the way to said substrate.

10. The trench DMOS transistor device of claim 1, wherein a plurality of deep regions is provided within said device.

11. The trench DMOS transistor device of claim 1, further comprising a metallic drain contact adjacent an upper surface of said deep region, a metallic source contact adjacent an upper surface of said source region, and a metallic gate contact adjacent an upper surface of said conductive region in a termination region remote from said source region.

12. The trench DMOS transistor device of claim 1, wherein said device comprises a plurality of transistor cells of square geometry or hexagonal geometry.

13. The trench DMOS transistor device of claim 1, wherein said trench DMOS transistor device is a silicon device.

14. The trench DMOS transistor device of claim 1, wherein said first insulating layer is an oxide layer.

15. The trench DMOS transistor device of claim 1, wherein the conductive region is a doped polycrystalline silicon region.

16. The trench DMOS transistor device of claim 1, wherein said first conductivity type is N-type conductivity and said second conductivity type is P-type conductivity.

17. The trench DMOS transistor device of claim 1, wherein said substrate is an N+ substrate, said epitaxial layer is an N epitaxial layer, said body region is a P region, and said source region is an N+ region.

18. A trench DMOS transistor device comprising:

a silicon substrate of N-type conductivity, said substrate acting as a drain region for said device;

a silicon epitaxial layer of said N-type conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

a silicon oxide insulating layer lining at least a portion of said trench;

a doped polycrystalline silicon conductive region within said trench adjacent said insulating layer;

a body region of P-type conductivity provided within an upper portion of said epitaxial layer and adjacent said trench;

a source region of N-type conductivity provided within an upper portion of said body region and adjacent said trench; and

a low resistivity deep region extending into said device from an upper surface of said epitaxial layer to said substrate,

said trench DMOS transistor device comprising a plurality of transistor cells provided with a common source contact, a common drain contact and a common gate contact, each provided on a top surface of said device.

19. The trench DMOS transistor device of claim 18, wherein said low resistivity deep region has a resistivity of 0.01 Ohm-cm or less.

20. The trench DMOS transistor device of claim 18, wherein said deep region comprises a semiconductor region of N-type conductivity.

21. The trench DMOS transistor device of claim 18, wherein said deep region comprises a metallic region.

22. The trench DMOS transistor device of claim 18, wherein said deep region comprises a doped polysilicon region.

23. The trench DMOS transistor device of claim 18, wherein said cells are provided in a geometry selected from a hexagonal geometry and a square geometry.

24. A method of forming a trench DMOS transistor device comprising:

providing a substrate of a first conductivity type, said substrate acting as a common drain region for said device;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer;

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench; and

forming a low resistivity deep region extending into said device from an upper surface of said epitaxial layer, said deep region acting to provide electrical contact with said substrate.

25. The method of claim 24, wherein said deep region comprises a semiconductor region of said first conductivity type that is formed by an implantation and diffusion process.

26. The method of claim24, wherein said deep region comprises a metallic region, and wherein said deep region is formed by a process comprising etching a deep trench that extends into said device from an upper surface of said epitaxial layer, and depositing metal within said deep trench.

27. The method of claim 24, wherein said deep region comprises a doped polysilicon region, and wherein said deep region is formed by a process comprising etching a deep trench that extends into said device from an upper surface of said epitaxial layer, and depositing polysilicon within said deep trench.

28. The method of claim 24, further comprising: forming a metallic drain contact adjacent an upper surface of said deep region, forming a metallic source contact adjacent an upper surface of said source region, and forming a metallic gate contact adjacent an upper surface of said conductive region in a termination region remote from said source region.

29. The method of claim 24, wherein said low resistivity deep region has a resistivity of 0.01 Ohm-cm or less and extends at least 20 % of the distance from said upper surface of said epitaxial layer to said substrate.

30. The method of claim 29, wherein said low resistivity deep region extends from said upper surface of said epitaxial layer to said substrate.